a memory controller for controlling data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits of data in parallel; and

a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, for transferring n bits of data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

means for forming n bits of data using said successive groups of m bits of data and supplying said n bits of data in parallel to said data processor through said second bus, and

a converter for converting said graphic data temporarily stored in said storage into serial data which is provided to said output means.

Please cancel claims 1-12, 14, 16 and 18-34 without prejudice or disclaimer of the matter therein.

Please add new claims 49-66 as follows:

~~49. A graphic processing apparatus comprising:~~

memory means for storing graphic data;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel,

wherein said memory controller includes:

storage means for temporarily storing graphic data read out from said memory means successively in a predetermined period of time via said first bus,

means for applying said temporarily stored graphic data to said data processing means as n-bit parallel data, and

converting means for converting said temporarily stored graphic data into serial data and outputting the serial data to said output means.

50. A graphic processing apparatus according to claim 49, wherein said memory controller includes multiplexer means for outputting n-bit graphic data transferred from said data processing means on said first bus having the m-bit width successively in a time-sharing manner.

51. A graphic processing apparatus according to claim 49, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

52. A graphic processing apparatus according to claim 50, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

53. A graphic processing apparatus according to claim 49, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory means designated by said data processing means.

54. A graphic processing apparatus according to claim 50, wherein graphic data to be transferred to said memory controller via said first bus are successively read out

plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory means designated by said data processing means.

55. A graphic processing apparatus according to claim 53, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

56. A graphic processing apparatus according to claim 54, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

57. A graphic processing apparatus comprising:

memory means for storing graphic data, said memory means being accessed by using a row address and a column address;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and n>m) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel; and

wherein said memory controller includes:

means for reading out a plurality of graphic data at different column addresses at a same row address from said memory means via said first bus successively in a predetermined period of time,

means for applying said read-out graphic data to said data processing means as n-bit parallel data, and

converting means for converting said read-out graphic data into serial data and outputting the serial data to said output means.

58. A graphic processing apparatus according to claim 57, wherein said memory controller includes means for successively generating a plurality of column addresses on the basis of a signal for accessing said memory means applied from said data processing means.

Sub F47 ~~59.~~ A memory controller for controlling transfer of data between memory means for storing graphic data and a

processor and between said memory means and display means, comprising:

m-bit terminals (wherein m is an integer) connected to said memory means, for transferring data of m bits successively in a predetermined period of time between said memory means and said memory controller;

an n-bit interface (wherein n is an integer and n>m) connected to said processor, for transferring data of n bits in parallel between said processor and said memory controller;

at least one bit terminal connected to said display means, for transferring serial data between said display means and said memory controller;

first converting means for performing conversion between data of plural sets of m bits via said m-bit terminals and data of n bits via said n-bit interface; and

second converting means for converting said data of plural sets of m bits via said m-bit terminals into said serial data.

10. ~~60.~~ A memory controller according to claim ~~59~~ 9, wherein data to be converted by said first converting means are read out plural times from said memory means within a transfer unit time successively in a predetermined period of time on the basis of addresses designated by said processor.

11. ~~61.~~ A memory controller according to claim ~~59~~ 9, wherein said first converting means includes storage means for

temporarily storing graphic data sent from said memory means via said m-bit terminals.

12. 9
~~62.~~ A memory controller according to claim ~~59~~, wherein said second converting means includes storage means for temporarily storing graphic data sent from said memory means via said m-bit terminals.

~~63.~~ A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and n>m);

storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

means for forming n bits of data by combining successive groups of m bits of data from said m bit terminals and supplying said n bits of data in parallel to said n bit terminals; and